## WHAT IS CLAIMED IS:

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- 1. A link bus between control chipsets, said control chipsets including a first control chip and a second control chip, said link bus comprising:
- a first address/data (AD) bus for transmitting address and data chiefly from said first control chip to said second control chip; and
  - a second address/data bus for transmitting address and data chiefly from said second control chip to said first control chip.
  - 2. The link bus of claim 1, wherein said first AD bus is a common bi-directional bus.
- 3. The link bus of claim 2, further comprising a first command signal line for transmitting a request signal to said second control chip from said first control chip.
- 4. The link bus of claim 2, wherein said first control chip has a higher priority in respect of controlling said first AD bus.
- 5. The link bus of claim 1, wherein said second AD bus is a common bi-directional bus.
  - 6. The link bus of claim 5, further comprising a second command signal line for transmitting a bus request signal to said first control chip from said second control chip.
  - 7. The link bus of claim 5, wherein said second control chip has a higher priority in respect of controlling said second AD bus.
  - 8. The link bus of claim 1, wherein said first control chip is a north bridge chip, and said second control chip is a south bridge chip.
  - 9. The link bus of claim 1, wherein said first control chip is a south bridge chip, and said second control chip is a north bridge chip.

10. A method for arbitration a link bus between control chipsets, said control chipsets including a first control chip, a second control chip, said link bus including a first address/data (AD) bus, and a second address/data bus, said method comprising:

transmitting address and data through said first AD bus from said first control chip to said second control chip;

transmitting a request from said first control chip to said second control chip when said first control chip needs said second AD bus;

holding said second AD bus if said second control chip is still transacting through said second AD bus; and

transmitting address and data from said first control chip to said second control chip through said second AD bus after a turn-around cycle if said second control chip doesn't need said second AD bus.

11. The method of claim 10, further comprising:

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transmitting a request signal from said second control chip, if said second control chip needs said second AD bus, when said first control chip is transacting through said second AD bus;

stopping transacting through said second AD bus; from said first control chip; and

transmitting address and data from said second control chip to said first control chip through said second AD bus after a turn-around cycle.

- 12. The method of claim 10, wherein said first control chip is a north bridge chip, and said second control chip is a south bridge chip.
- 13. The method of claim 10, wherein said first control chip is a south bridge chip, and said second control chip is a north bridge chip.

14. An arbitration method of a link bus between control chipsets, said control chipsets including a first control chip, and a second control chip, said link bus including a first address/data (AD) bus, and a second address/data bus, said arbitration method comprising:

controlling said second AD bus to transmit address and data from said second control chip to said first control chip;

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transmitting a request from said second control chip to said first control chip when said second control chip needs said first AD bus;

holding said first AD bus if said first control chip is still controlling said first

10 AD bus; and

controlling said first AD bus to transmit address and data from said second control chip to said first control chip after a turn-around cycle if said first control chip doesn't need said first AD bus.

15. The arbitration method of claim 14, further comprising:

transmitting a request signal from said first control chip, if said first control chip needs said first AD bus, when said second control chip is still controlling said first AD bus;

stopping controlling said first AD bus from said second control chip; and controlling said first AD bus to transmit address and data from said first control chip to said second control chip after a turn-around cycle.

- 16. The arbitration method of claim 14, wherein said first control chip is a north bridge chip, and said second control chip is a south bridge chip.
- 17. The arbitration method of claim 14, wherein said first control chip is a south bridge chip, and said second control chip is a north bridge chip.